ABSTRACT OF THE DISCLOSURE

In the data recovery circuit of the invention, a first group of sampling clock pulses is used for sampling approximately the central portions of the data bits in an incoming data stream to produce a first sampled data stream, while a second group of sampling clock pulses is used for sampling approximately the transition portions between every two adjacent data bits in the incoming data stream to produce a second sampled data stream. By detecting the resemblance of each bit in the second sampled data stream to the corresponding two adjacent bits in the first sampled data stream, a phase detection and correction circuit determines an early condition or a late condition for the phases of the sampling clocks and produces a signal to correct the phases of the sampling clocks by shifting the phases backwards or forwards. According to the invention, sampling clocks with lower frequencies can be used for sampling, and the phase error can be corrected to obtain the correct data recovery.